

REMARKS/ARGUMENTS

Upon entry of this amendment, which amends claims 1, 15, 24 and 33, claims 1-41 remain pending. Support for all amended claims can be found in the specification, and no new matter has been added.

In the Office Action to which this paper is responsive, claims 1-9, 11-21, 23-25, 33 and 34 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greene, U.S. Patent No. 5,929,872, in view of Sturgess, U.S. Patent No. 5,861,893. Claims 10-14 and 22-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greene in view of Sturgess (as applied to claims 1 and 15) and further in view of Marino, U.S. Patent No. 6,784,893. Claims 26-32 and 35-41 were objected to as being dependent on a rejected base claim, but were found to be allowable if rewritten in independent form.

Reconsideration in view of the foregoing amendments and following remarks is respectfully requested.

Rejection of claims 1-9, 11-21, 23-25, 33 and 34 under 35 U.S.C. §103(a)

Claims 1-9, 11-21, 23-25, 33 and 34 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greene, U.S. Patent No. 5,929,872, in view of Sturgess, U.S. Patent No. 5,861,893. Applicants respectfully traverse.

Claim 1 in the present application (as amended) is directed to a method of self-programming a GPU, in which a blit instruction is received from the CPU, “wherein a destination for the blit operation corresponds to a control register,” and the blit operation is used to store a first control value in the control register; the control value in the control register determines a behavior of the GPU. The use of a blit operation to store a control value in a control register is not taught or suggested by the combination of Greene and Sturgess.

Greene discloses a “Blt accelerator” that speeds up performance of a sequence of block transfer (“blit,” or “Blt”) operations by storing intermediate results in a temporary storage unit (Greene, Abstract). As shown in Fig. 1, a host loads parameters of a blit operation (source location, destination location, block size, operation to be performed) into control registers (16) (col. 3, lines 2-3), and the Blt accelerator (10) reads the registers and performs the operation.

The source of the data for the blit operation is a display memory (14) or a temporary storage unit (22), and the final result is written back to the display memory 14 and/or the temporary storage unit 22 (col. 3, lines 8-18). While Greene indicates that a blit engine might read a control register (i.e., a register that stores a control value that determines a behavior of a processor), Greene does not disclose or suggest that a destination of the blit operation could correspond to a control register. Instead, Greene describes only blit operations that are performed on pixel data and generate modified pixel data that is ultimately stored in the display memory.

Sturgess discloses a blit ("BLTBIT") engine that arbitrates among requests for blits by different clients of a graphics system (e.g., operating system and various application programs that use 2-D and/or 3-D graphics pipelines). The BLTBIT engine determines the order in which such requests are handled, allowing blit requests initiated by the operating-system to take priority over blit requests initiated by application programs. (Sturgess, Abstract). Sturgess describes a blit (block transfer) operation implemented by the BLTBIT engine as "transferring data blocks between different surfaces of graphics memory 160" (col. 5, lines 31-38) and, like Greene, does not disclose or even suggest that the BLTBIT engine might be used to store values anywhere other than in graphics memory, let alone that the destination of a blit operation could correspond to a control register as recited in claim 1.

Thus, nothing in the combination of Greene and Sturgess fairly suggests self-programming a GPU by using a blit operation for which the destination corresponds to a control register of the GPU.

For at least these reasons, claim 1 is patentable over Green and Sturgess. Claims 2-9 and 11-14 depend from claim 1 and derive patentability therefrom.

Independent claim 15, as amended, recites a graphics rendering system comprising a graphics processing unit having a control register and a blit engine; the blit engine is "adapted to perform a blit operation that stores a first control value in the control register" in response to a command from a CPU. As discussed above, neither Greene nor Sturgess nor any combination thereof discloses or suggests that a blit operation could be used to store a control value in a control register.

For at least this reason, claim 15 is patentable over Greene and Sturgess. Claims 16-21 and 23 depend from claim 15 and derive patentability therefrom.

Independent claim 24, as amended, recites a method of self-programming a GPU that includes, inter alia, "writing a set of self-programming commands including a blit instruction to the command buffer, wherein a destination for the blit instruction corresponds to a control register of the GPU." As discussed above with reference to claim 1, neither Greene nor Sturgess nor any combination thereof discloses or suggests that a blit instruction where the destination corresponds to a control register.

For at least this reason, claim 24 is patentable over Greene and Sturgess. Claim 25 depends from claim 24 and derives patentability therefrom.

Independent claim 33, as amended, recites an information storage medium having a set of instructions for directing an information processing device to, inter alia, write "a set of self-programming commands including a blit instruction to the command buffer, wherein a destination for the blit instruction corresponds to a control register of the GPU." As discussed above with reference to claim 1, neither Greene nor Sturgess nor any combination thereof discloses or suggests that a blit instruction where the destination corresponds to a control register.

For at least this reason, claim 33 is patentable over Greene and Sturgess. Claim 34 depends from claim 33 and derives patentability therefrom.

In view of the foregoing, withdrawal of the rejection of claims 1-9, 11-21, 23-25, 33 and 34 under 35 U.S.C. §103(a) is respectfully requested.

Rejection of Claims 10-14 and 22-23 under 35 U.S.C. §103(a)

Claims 10-14 and 22-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Greene in view of Sturgess (as applied to claims 1 and 15) and further in view of Marino, U.S. Patent No. 6,784,893. Marino was relied on for the additional element of a "colorkey" operation recited in claims 10 and 22.

Claims 10-14 depend from claim 1, and claims 22 and 23 depend from claim 15. As discussed above, the rejection of claims 1 and 15 over Greene and Sturgess cannot properly

be maintained. Further, like Greene and Sturgess, Marino also fails to disclose or suggest that a destination of [a] blit operation could correspond to a control register as recited in claim 1 or that a blit engine could be adapted to perform a blit operation that stores a first control value in a control register as recited in claim 15; Marino instead states that the rasterop unit operates on pixel data and "has resulting pixel data 64 as its only output" (col. 3, lines 46-55).

Thus, the combination of Greene, Sturgess and Marino fails to render obvious the subject matter of base claims 1 and 15, let alone that of dependent claims 10-14, 22 and 23. Withdrawal of the rejection of claims 10-14, 22 and 23 under 35 U.S.C. §103(a) is respectfully requested.

Objection to Claims 26-32 and 35-41

Claims 26-32 and 35-41 were objected to as being dependent on a rejected base claim, but were found to be allowable if rewritten in independent form. In view of the foregoing arguments and amendments with regard to base claims 24 and 33, Applicants respectfully submit that claims 26-32 and 35-41 are in condition for allowance without being rewritten in independent form. Withdrawal of the objection is respectfully requested.

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PATENT

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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